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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,862	08/18/2003	Vivek V. Gupta	VRT0092US	3308

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EXAMINER

PATEL, HETUL B

ART UNIT PAPER NUMBER

2186

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,862	GUPTA ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-35 are presented for examination.

Claim Objections

2. Claims 1, 4, 27, 30 and 33 are objected to because of the following informalities:

It should be stated as "... cloning information stored in a first unit of storage into a second unit of storage, ..." instead of "... cloning information stored in a first unit of storage in a second unit of storage, ..." as disclosed in claims 1, 27, 30 and 33 of this application.

The phrase "... said second unit of storage to said unit of storage of said storage unit ..." of claim 4 is not clear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4 and 6 recite the limitation "said unit of storage" in them. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3-35 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kashima et al. (USPN: 5,485,598) hereinafter, Kashima.

As per claim 1, Kashima teaches a method comprising cloning/copying information stored in a first unit of storage (the first cache memory) in a second unit of storage (the second cache memory), wherein said first unit of storage is stored in a first cache maintained by an upper-level system, and said second unit of storage is stored in a second cache (e.g. see the abstract).

As per claim 3, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprises copying said information from said first unit of storage to said second unit of storage (e.g. see the abstract).

As per claim 4, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- partially writing a unit of storage (i.e. a portion of data from the first cache) of a storage unit (i.e. the first cache) by writing a portion of said information (i.e.

a portion of data from the first cache) from said second unit of storage (i.e. a portion of data from the second cache) to said unit of storage of said storage unit; and

- partially writing said unit of storage of said storage unit by writing new information (i.e. renewed data of the first cache) to said unit of storage of said storage unit (e.g. see the abstract).

As per claim 5, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said copying comprises:

- reading said information (i.e. the old data of the first cache) from said first unit of storage (i.e. the first cache); and
- writing said information (i.e. the old data of the first cache) to said second unit of storage (i.e. the second cache) (e.g. see the abstract).

As per claim 6, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising writing to said unit of storage after said reading, i.e. the old data is written/stored into the second cache after being read from the first cache (e.g. see the abstract).

As per claim 7, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- reading said information (i.e. the old data) from said second unit of storage (i.e. from the second cache); and

- calculating parity information using said information, i.e. calculating new CK/parity data using the old data, the new data and the new CK data (e.g. see the abstract).

As per claims 8 and 9, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising:

- determining if said first unit of storage (the first cache) is to be modified, i.e. the new data to be written to the first cache; and
- performing said cloning (i.e. copying) if said first unit of storage is to be modified, i.e. if determined that the new data needs to be written to the first cache, then copying the old/existing data from the first cache into the second cache (e.g. see the abstract).

As per claim 10, see arguments with respect to the rejection of claim 7. Claim 10 is also rejected based on the same rationale as the rejection of claim 10.

As per claims 11 and 12, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the method further comprising modifying said first unit of storage after said performing said cloning, i.e. writing new data into the first cache after copying old data from the first cache into the second cache (e.g. see the abstract).

As per claim 13, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said cloning comprising determining if said information will be needed in the future; and performing said cloning if said information will be needed in the future, i.e. if the old data is going to be renewed by the new data in

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the first cache, then cloning/copying process is performed since the old data may be needed in future if the new data is lost/corrupted for any reason(s) (e.g. see the abstract).

As per claim 14, Kashima teaches a storage system (i.e. 10 in Fig. 8) comprising an old data cache (i.e. the first cache, 17 in Fig. 8) (e.g. see Fig. 8).

As per claim 15, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising:

- an upper-level system (i.e. 10 in Fig. 8), communicatively coupled to said old data cache (i.e. 17 in Fig. 8); and
- a lower-level storage module (i.e. the disk array device, 1 in Fig. 8), communicatively coupled to said old data cache and said upper-level system (e.g. see Fig. 8).

As per claim 16, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module is a volume manager (i.e. the RAID disk array, 1 in Fig. 8).

As per claim 17, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module comprises a cache (i.e. the old CK data cache, 16 in Fig. 8).

As per claim 18, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module is configured to clone/copy information from a page in said cache (i.e. the old CK data cache, 16 in Fig.

8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 19, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system (i.e. 10 in Fig. 8) is configured to access said page in said old data cache (i.e. 17 in Fig. 8).

As per claim 20, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system comprises a cache (i.e. the disk cache, 13 in Fig. 8).

As per claim 21, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is configured to clone/copy information from a page in said cache (i.e. the disk cache, 13 in Fig. 8) to a page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 22, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said lower-level storage module (i.e. the disk array device, 1 in Fig. 8) is configured to access said page in said old data cache (i.e. 17 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 23, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said upper-level system is a hardware RAID controller since RAID (i.e. 1 in Fig. 8) is controlled by the upper-level system (i.e. the computer, 10 in Fig. 8, specifically the CPU, 11 in Fig. 8) (e.g. see Fig. 8).

As per claim 24, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising storage unit (i.e. disks, 2a-2d in Fig. 8), wherein said lower-level storage module (i.e. 16 in Fig. 8) is coupled to control said storage unit (e.g. see fig. 8).

As per claim 25, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that the system further comprising a parity cache (i.e. the old CK data cache, 16 in Fig. 8), wherein said storage unit is a RAID (i.e. 2a-2d in Fig. 8), and said parity cache is configured to store parity information corresponding to data read from said RAID (e.g. see the claim 18).

As per claim 26, Kashima teaches the claimed invention as described above and furthermore, Kashima teaches that said storage unit (i.e. the main memory, 12 in Fig. 8) comprises a source volume (i.e. 17 in Fig. 8) and a snapshot volume (i.e. 13 in Fig. 8), and said lower-level storage module (i.e. 1 in Fig. 8) is configured to write information from a page in said old data cache (i.e. 17 in Fig. 8) to said snapshot volume (i.e. 13 in Fig. 8) (e.g. see Col. 5, lines 13-25, the abstract and the Fig. 8).

As per claim 30, Kashima teaches a storage system comprising:

- a processor (i.e. the CPU 11 in Fig. 8);
- computer readable medium coupled to said processor; and computer code, encoded in said computer readable medium, configured to cause said processor to, (i.e. this feature is inherently embedded in the system taught by Kashima):

- clone/copy information stored into a first unit of storage (the first cache)
into a second unit of storage (the second cache), wherein
 - said first unit of storage is stored in a first cache (i.e. 17 in Fig. 8) maintained by an upper-level system (i.e. 10 in Fig. 8), and
 - said second unit of storage is stored in a second cache (e.g. see Fig. 8 and the abstract).

As per claim 31, see arguments with respect to the rejection of claims 30 and 4. Claim 31 is also rejected based on the same rationale as the rejection of claims 30 and 4.

As per claim 32, see arguments with respect to the rejection of claims 30 and 5-6. Claim 32 is also rejected based on the same rationale as the rejection of claims 30 and 5-6.

As per claims 27-29, see arguments with respect to the rejection of claims 30-32, respectively. Claims 27-29 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

As per claims 33-35, see arguments with respect to the rejection of claims 30-32, respectively. Claims 33-35 are also rejected based on the same rationale as the rejection of claims 30-32, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashima.

As per claim 2, Kashima teaches the claimed invention as described above.

Official notice is taken of the prior art teaching a single cache comprising a plurality of caches. First of all, it has been held that to make integral is not generally given patentable weight. Note In re Larson 144 USPQ 347 (CCPA 1965). Furthermore In re Tomoyuki Kohno 157 USPQ 275 (CCPA 1968) states that to integrate electrical components onto a unitary, one piece structure would be obvious. Integrating multiple components on a single chip reduces cabling problems, reduces latency required for communicating among multiple components, improves efficiency of message passing, reduces chip-to-chip communications costs, allows for less pin count, area saving and high speed data transfer between the elements and leads to further power efficiency and increased scalability. Because multiple caches integrated on a single cache (chip) provides improvements in efficiency, cost and scalability over individual caches, it would have been obvious to comprise a plurality of caches on a single cache. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER